supplying free abrasive grains to said fixed abrasive grains; and

subsequently grinding said surface of a semiconductor wafer with said fixed abrasive grains and said free abrasive grains. --

-- 6. The method of claim 5, wherein said fixed abrasive grains have a larger diameter than said free abrasive grains. --

-- 7. The method of claim 5, wherein grinding includes both sides grinding of a semiconductor wafer or grinding of a chamfered portion. --

-- 8. The method of claim 6, wherein grinding includes both sides grinding of a semiconductor wafer or grinding of a chamfered portion. --

REMARKS

Claims 1-4 are pending in this application and have been rejected under 35 USC 112, second paragraph, and 35 USC 102(a). Claims 1-4 have been cancelled and claims 5-8 have been added. The newly added claims are directed to a process for grinding the surface of a semiconductor wafer and recite 1) grinding a surface of a semiconductor wafer with fixed abrasive grains; 2) supplying free abrasive grains; and 3) subsequently grinding the semiconductor surface with fixed abrasive grains and free abrasive grains. Because the newly added claims clarify that the subsequent grinding both employs free and fixed abrasive grains and does not use the phrase "the same grinding axis", the rejections of claims 1-4 under 35 USC 112, second paragraph, are moot in view of the newly added claims.

Additionally, the prior art of record does not disclose the limitations of claims 5-8 (corresponding to claims 1-4, now canceled). Sato discloses a process wherein fixed and free abrasive grains are used in a two-step grinding process, with the second step using smaller-sized abrasive grains. Sato does not teach, disclose, or suggest the use of a two-step grinding process wherein the first step is carried out by only fixed abrasive grains and the second step by a combination of both fixed and free abrasive grains. Rather, Sato discloses a wafer grinding method, which employs both fixed abrasive grains 13, fixed to a polishing pad 12, and free abrasive grains 15 intervening between the polishing pad 12 and a work 10. Furthermore, Sato discloses a two step process of repeating such wafer grinding methods by changing the size of the abrasive grains.

This present invention, on the other hand, discloses a method using a grinding (via, for example, a stone). Unlike Sato, which uses abrasive grains in the first and second step, the present invention uses fixed abrasive grains during grinding, and a combination of fixed abrasive and free abrasive grains in the subsequent grinding. For at least this reason, the rejection of claims 1-4 (corresponding to newly added claims 5-8) is respectfully traversed.

All claims are now in condition for allowance and a notice thereof is earnestly solicited.

Attached hereto is a marked up version of the changes made to the claims by the current amendment. The attached page is captioned "**VERSION WITH MARKINGS TO SHOW CHANGES MADE**".

In the unlikely event that the transmittal letter is separated from this document and the Patent Office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to

Deposit Account No. 03-1952 referencing docket no. 47408200700 However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Respectfully submitted,

Dated: September 24, 2001

By: _____
Kevin R. Spivak
Registration No. 43,148

Morrison & Foerster LLP
2000 Pennsylvania Avenue, N.W.
Washington, D.C. 20006-1888
Telephone: (202) 887-6924
Facsimile: (202) 263-8396

VERSION WITH MARKINGS TO SHOW CHANGES MADE

Please cancel claims 1-4 without prejudice or disclaimer.

Please add the following new claims:

5. A method for grinding semiconductor wafers comprising:

grinding a surface of a semiconductor wafer with fixed abrasive grains;

supplying free abrasive grains to said fixed abrasive grains; and

subsequently grinding said surface of a semiconductor wafer with said fixed abrasive grains and said free abrasive grains.

6. The method of claim 5, wherein said fixed abrasive grains have a larger diameter than said free abrasive grains.

7. The method of claim 5, wherein grinding includes both sides grinding of a semiconductor wafer or grinding of a chamfered portion.

8. The method of claim 6, wherein grinding includes both sides grinding of a semiconductor wafer or grinding of a chamfered portion.